# LC-Ladder Filters Emulated by Circuits with Current Controlled Conveyors and Grounded Capacitors

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***Abstract*— The paper implements the well-known leapfrog method of LC-ladder filters simulation by circuits employing only multiple outputs second-generation current controlled conveyors (MO-CCCII) and grounded capacitors. The proposed method is general, because on a hand it implements any type of frequency response and on the other side both all pole and finite-transmission-zeros passive filters are emulated. Using current controlled devices, the circuits are electronically tunable and do not require any matching constraints, making the approach extremely convenient for systematic design and dense layout. SPICE simulations made with circuits employing bipolar MO-CCCII demonstrate the validity of the approach.**

## I. INTRODUCTION

Over the last decade or so, current-mode (CM) filters using second-generation current conveyors (CCII) have received considerable attention owing to the fact that their bandwidth, linearity, and dynamic range performances are better than those of their op-amp based counterparts [1]-[3]. In many cases, the current conveyors simplifies design in much same way as the op-amps, but they present alternative ways for implementing analog systems. It resulted in new methods which implement analog transfer functions, giving advantages over voltage op-amp counterparts in terms of accuracy, bandwidth, convenience and simpler circuits.

With recently introduced second-generation current controlled conveyors (CCCII) [4], current conveyors' applications have been extended to the domain of electronically adjustable functions. Electronic adjustability is attributed to intrinsic resistance ($R_X$) at port X which depends on bias current $I_o$. Recently, designs of current controlled conveyors based filters using multiple outputs CCCII (MO-CCCII) [3], [5], alleviate considerably the design of multi-loop filters. These devices have two or more high impedance positive/negative outputs and will be used in our designs.

This paper presents a general design method for CM ladder filters using only MO-CCCII and grounded capacitors. The method is based on operational simulation of RLC ladder prototypes. These active implementations share all the low sensitivity characteristics and low component spread of passive filter prototypes. These advantages are totally preserved in CM ladder active filter designs [6], [7].

Even if the technique of simulating LC-ladder filters by their signal-flow graphs is very well established in the area of all-pole lowpass filters, our approach based on a systematic design procedure extends the applicability of leapfrog method to all types of passive networks configurations. The design procedure, designated by us as *Active Synthesis of Ladder Network Immitances,* was developped by Schaumann [8], [9] for voltage mode ***T**ransconductor-**G**rounded **C**apacitor* (TGC) circuits and, as is shown in the paper, it can be successfully extended to the case of multi-output CM circuits.

The Schaumann approach is very methodical and simple to implement, attributes retained also in our MO-CCCII implementation. It synthetize in our case, by simple and repetitive operations, the admittance/impedance of each arm of the passive network as a CM transfer function. As consequence, we are capable to emulate any passive ladder filter network configuration, that justify the general character of the method. To demonstrate the validity of active synthesis method, two design examples are presented, revealing some of the problems that arise during the synthesis process, due to the non-ideal character of bipolar devices used as current conveyors.

## II. BIPOLAR DO-CCCII DESCRIPTION

A DO-CCCII or CCCII± is a MO-CCCII with only two output terminals (Fig. 1(a)). The ± sign indicates the output currents are in opposite direction. The ideal relationship between terminal currents and voltages is defined as:

$$\begin{bmatrix} V_X \\ I_Y \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 1 & R_o & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \quad (1)$$

$I_X, I_Y, I_{Z+}, I_{Z-}$ and $V_X, V_Y, V_{Z+}, V_{Z-}$ in (1) denote currents respectively voltages at DO-CCCII terminals. By convention, a positive current indicates that the current flows in the device. $R_o$ in (1) represents the input resistance at port X. For bipolar CCCII, the resistance is $R_o = V_T/(2I_0)$, where $I_0$ is the bias current of the conveyor and $V_T$ is roughly 26mV at room temperature [4].

In an usual application, the current conveyor is used as a transconductance amplifier. The terminal X is grounded and the voltage input signal is $V_Y$, the output currents being given by

$$I_{Z\pm} = \mp V_Y / R_0 \quad (2)$$

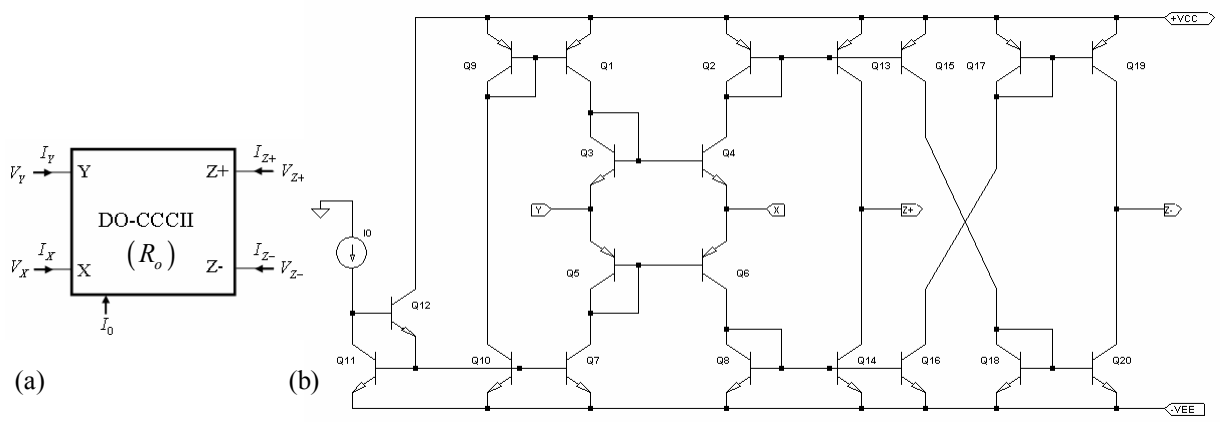


Figure 1. (a) Block diagram of the dual-output second generation current conveyor (DO-CCII), (b) Schematic implementation of DO-CCCII using BJT.

If X becomes the input terminal and the port Y is grounded then the device acts as a current mirror with $R_o$ as input resistance.

In order to estimate the correctness of the method and to evaluate the frequency domain performances of proposed circuits, we used the bipolar realization in Fig. 1(b)[10]. The DC supply voltages are ±2.5V and the PNP and NPN transistors use the parameters of PR100N and NR100N bipolar transistors arrays [3].

A multi-output CCCII (MO-CCCII) has more than the two outputs of DO-CCCII, usually two ($I_{Z1+}$ and $I_{Z2+}$) instead of $I_{Z+}$ and other two ($I_{Z1-}$ and $I_{Z2-}$) instead of $I_{Z-}$. All these outputs maintain ideally the same properties as the corresponding outputs of DO-CCCII, being obtained by current mirroring. Only the necessities of circuit synthesis dictates the number of outputs of a MO-CCCII.

## III. Active Synthesis Methods

### A. Leapfrog Synthesis Procedures

As shown in Fig. 2(a), an LC-ladder filter network can be characterized by the admittance blocks in the series arms and impedance blocks in the parallel arms. This representation leads to the corresponding signal-flow graph of Fig. 2(b) in terms of node voltages ($v_i, v_2, v_4 \ldots$) and mesh currents ($i_1, i_3, i_5 \ldots$).

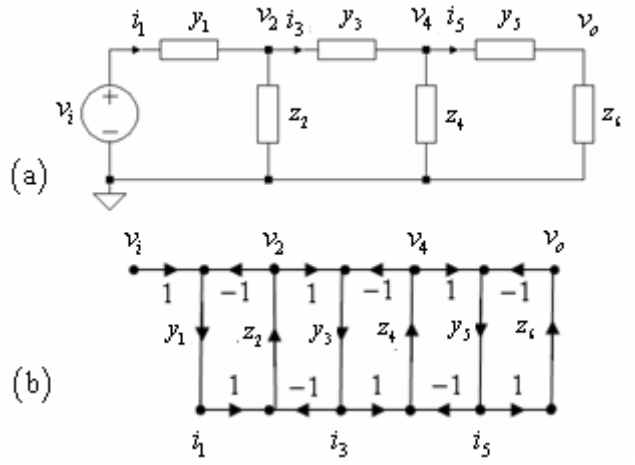


Figure 2. (a) General LC-ladder filter schematic (b) Its signal-flow graph.

In our disscusion throughout the paper, all RLC prototypes circuits are assumed to be normalized with respect to impedance level. Therefore the parameters and variables are dimensionless, the transmittances $z_k$ and $y_j$ in Fig. 2(b) are current transfer functions and $v_k$ is to be interpreted as a current signal regardless of notation. Any circuit realizing the same signal-flow graph as the LC-ladder filter independent of node variable names obviously realizes the same current transfer function. Thus, the design is reduced to the synthesis of active filter subcircuits that simulate the normalized immitance functions of RLC circuits (the transmittances in the graph) by current transfer functions. The synthesized circuit will implement also the subtractions in the nodes of the graph by using the opposite sign outputs of MO-CCCII circuits.

### B. Active Synthesis of One-port Immitances

In this paper, the current summers and current transfer functions of $Z_k$ and $Y_j$ are synthesized using MO-CCCII circuits and grounded capacitors. The basic circuit is built around a DO-CCCII and a grounded admittance as Fig. 3 shows, and its current transfer functions emulates completely the operations realized across a node in the graph in Fig. 1(b):

$$I_j = \frac{1}{R_o Y_j}\left(I_{j-1} + I_{j+1}\right) \tag{3}$$

In a practical LC-ladder filter, the circuit branches shown in Fig. 1(a) typically consist of series and parallel combinations of inductors, capacitors and possibly resistors. In general, the branch immitances functions $y_i$ and $z_i$ of the RLC oneports

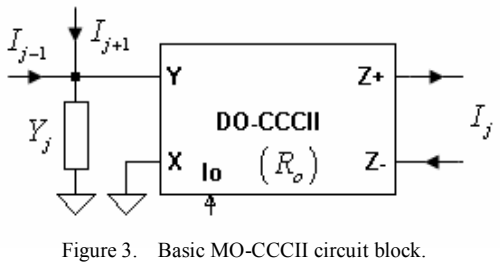


Figure 3. Basic MO-CCCII circuit block.

under consideration can be mathematically expressed in the form of a continuous fraction expansion:

$$F(s) = k_{01}^r s + k_{01}^c + \cfrac{1}{k_{02}^r s + k_{02}^c + \cfrac{1}{k_{11}^r s + k_{11}^c + \cfrac{1}{k_{12}^r s + k_{12}^c + \cfrac{1}{k_{21}^r s + k_{21}^c + \cfrac{1}{k_{22}^r s + k_{22}^c + \cfrac{1}{\cdots}}}}}} \quad (4)$$

where $k_{ij}^r$ and $k_{ij}^c$ are real positive constants that correspond to inductor/capacitor and resistor/conductor, respectively depending on the position in the original network. In the same way, $F(s)$ represents the impedance/admittance of a parallel/series branch of the ladder. The expression (4) is general and some coefficients may be zero or infinity depending on the particular case.

The main goal of this paper is to prove the possibility to implement $F(s)$ in (4) by CM circuits containing grounded capacitors and MO-CCCII. On this basis resides the general nature of CM leapfrog procedure developped in this paper.

The realization of $F(s)$ in (4) as a current transfer function implies the possibility to perform repeatedly in the implementing circuit the mathematical operations involved in writing the expression: addition and inversion. These operations are executed on two fundamental circuit structures presented in Fig. 4(a) and (b). The transfer function of circuit in Fig. 4(a) is inverse proportional with $s$ while the circuits in Fig. 4(b) are used to implement the equivalent of a grounded resistor of unity value or a unitary CM transfer function. If a different value resistor must to be implemented, a second CCCII circuit is needed, as will be shown further down. In this case, the value of the resistor dictates the bias current ratio of conveyors.

As is obvious from our previous statements, the MO-CCCII-grounded capacitors circuits elements are important not only for their CM transfer function but also for the input admittance, the inverse of the first function. Addition of two or more admittances ensued by inversion as current transfer function is given quite simply by the circuit in Fig. 4(c). Finally, Fig. 4(d) presents the way used to invert the input admittance or the CM transfer function. As a conclusion, the active synthesis of a RLC immitance is made using the fundamental admittances presented in Fig. 4(a) and (b) and alternating the operations of addition and inversion shown in Fig. 4(c) and (d) performed with the object to implement the continuous fraction expansion of the one-port immitance in (4) by a current transfer function.

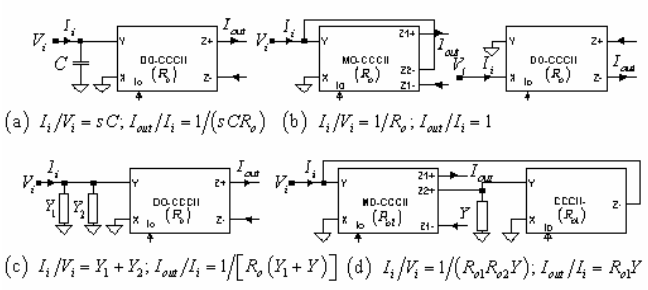


Figure 4. Fundamental circuit structures implementing (a) a grounded capacitor and (b) a constant. Realization of a CM transfer function by (c) addition and (d) inversion.

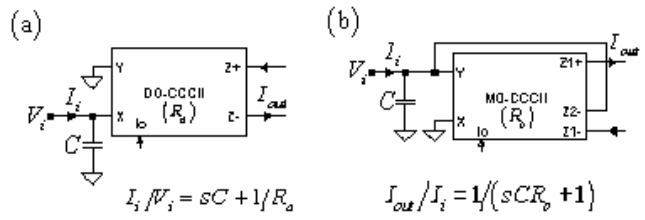


Figure 5. First order current transfer function circuits implemented by active synthesis procedures of one-port immitance.

Fig. 5 (a) and (b) illustrates a simple application of synthesis procedures. The first-order current transfer function of this case is the inverse of the sum of two fundamental admittances: a grounded capacitor and a grounded conductance represented by one of the circuits represented in Fig. 4(b). Both circuits present very similar frequency characteristics, with a slight advantage for the circuit in Fig. 5(a). Fig. 5(b) is a good example for the benefits of the use of multi-outputs current conveyors in active synthesis of one-port immitances. In place of two current conveyors, the first one needed to implement the active conductance and the second one to realize the addition of two conductances, it uses a single MO-CCCII to emulate both actions.

## IV. Design Example

The design procedure of an MO-CCCII with grounded capacitors filter starts by the selection of an appropiate RLC ladder prototype normalized with respect to both the frequency and impedance level. Next, the transmittances of each of the ladder arms of the circuits are established. In the next step, each transfer function is synthesized as an active CM circuit by the procedures introduced in Section III. Then, the subcircuits are interconnected in accordance with passive filter SFG. In the last step, a frequency denormalization is made in order to achieve the prescribed frequency behaviour.

To illustrate the versatility of the design procedures but also the limitations of employed bipolar conveyor, a third-order elliptic low-pass filter design example is given next.

The third-order elliptic low-pass LC-ladder prototype filter is given in Fig. 6(a). The circuit description in term of node voltages and mesh currents represents the starting point of the

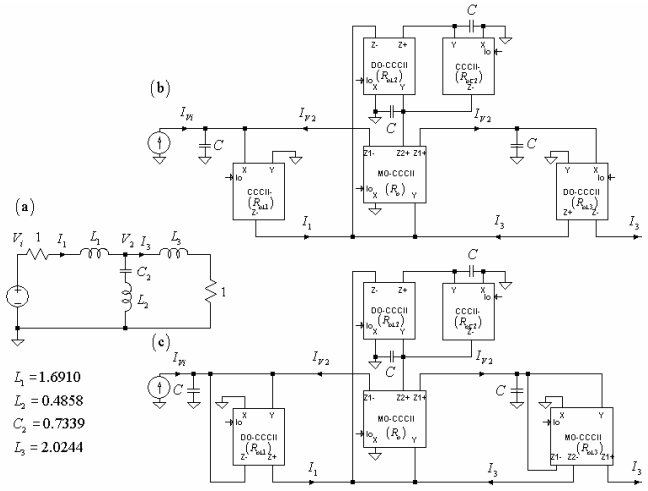


Figure 6. (a) Third-order elliptic low-pass LC-ladder prototype filter. (b) and (c) two MO-CCCII-grounded capacitors filter simulations of the passive ladder in (a)

active emulation of the passive network:

$$I_1 = \frac{1}{sL_1 + 1}(V_i - V_2), \tag{5}$$

$$V_2 = \left(sL_2 + \frac{1}{sC_2}\right)(I_1 - I_3) \tag{6}$$

$$I_3 = \frac{1}{sL_3 + 1}V_2 \tag{7}$$

In an active CM emulation all variables in (5)-(7) becomes currents, therefore, $I_{Vi}$ will replace $V_i$ and $I_{V2}$ wil take the place of $V_2$.

The design of the active filter consists of synthesizing the subcircuits that simulate the transmittances in (5)-(7). For the first and last equation, the solution was given in the earlier example from Fig. 5. To compare the performances, we used both solutions to realize the circuits in Fig. 6(b) and Fig. 6(c). In the first case, the unity constant is given by the finite input resistance at port X, in the second case it is obtained by the negative feedback at port Y. To implement the second equation, two inversions and one addition are needed, operations performed by three current conveyors and two capacitors.Viewing the passive and the active circuits in Fig. 6 it is convenient to understand the synthesis process.

Since the ratio between the largest and smallest reactance is relatively low in this example, we imposed a single value for all the capacitances in the active circuits ($C = 1nF$) and used the bias currents of CCCII devices to obtain the desired values of reactances. For a denormalized value $L_i$ of an inductance in the passive network of Fig. 6(a), the corresponding bias current in the active circuit is

$$I_{oLi} = \frac{V_T C}{2L_i} \tag{8}$$

The relation is unchanged if a capacitor $C_j$ takes the place of the inductor. For a corner frequency of 100kHz, the parameters

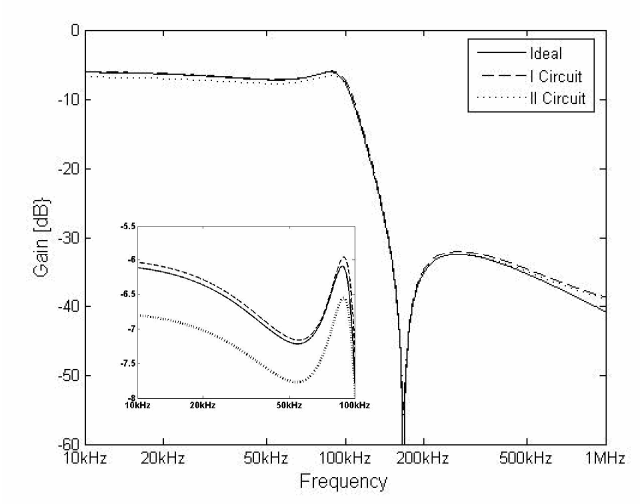


Figure 7. Ideal and simulated magnitude characteristics of third-order elliptic low-pass MO-CCCII filters in Fig. 6(b) and Fig. 6(c).

of active elements in Fig. 6(b) and (c) are: $I_{oL1} = 4.83\mu A$, $I_o = 15\mu A$, $I_{oL2} = 16.81\mu A$, $I_{oC2} = 11.13\mu A$, and $I_{oL3} = 4.04\mu A$.

Both ideal and simulated frequency responses of circuits in Fig. 6 are shown in Fig. 7. Besides a good concordance with the theory, two conclusions arise. Above all, the implementation of the first order transfer function in Fig. 5(a) gives better results than the circuit in Fig. 5(b), revealing the effect of the finite input impedance at the port Y. Then, the difference in the high frequency region comes from the non-ideal gains and parasitic impedances of current devices.

## V. CONCLUSIONS

The main goal of this paper was the developpment of general simulation method of LC-ladder filtres by active CM circuits containing only multi-output second generation current conveyors (MO-CCCII) and grounded capacitors. The method particularizes to the case of CM circuits different special techniques available in literature [8], [9]. The active circuits use exactly one capacitor for each reactance in the originating LC-ladder and maintain the number of active circuits employed at a minimum.

The validity of the design procedure was proved on some non-trivial design examples using bipolar current controlled conveyors as simulation vehicles. The deviations from ideal behaviour stem from the non-ideal performances of the bipolar devices and can be reduced by the use of better devices and active compensation techniques.

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